CLAIMS

WHAT IS CLAIMED IS:

1. A method, comprising:

providing a device having a dielectric layer;

applying a plurality of constant voltage pulses to said device; and

determining a time-to-breakdown for said dielectric layer based upon a number of pulses applied to said device until said dielectric layer breaks down.

2. The method of claim 1, further comprising measuring a current through said dielectric layer after one or more of said constant voltage pulses has been applied.

3. The method of claim 1, further comprising measuring a current through said dielectric layer after each of said plurality of constant voltage pulses has been applied.

4. The method of claim 1, wherein said time-to-breakdown is determined based upon a measurement of current flowing through said dielectric layer, said current being measured after one or more of said constant voltage pulses has been applied.

5. The method of claim 1, wherein said device is comprised of at least one of a transistor, a capacitor, a resistor and a memory cell.

6. The method of claim 1, wherein said dielectric layer is comprised of silicon dioxide or a material having a dielectric constant greater than 5.

7. The method of claim 1, wherein said constant voltage pulses have a voltage that ranges from approximately 4-5 volts.

8. The method of claim 1, wherein said pulses have a constant pulse width.

9. The method of claim 1, wherein said pulses have a constant pulse width of less than 1 μsec.

10. The method of claim 1, wherein said pulses have a constant pulse width of approximately 100 ns.

11. The method of claim 2 or 3, wherein said step of measuring said current through said dielectric layer is performed using an applied voltage of approximately 1-2 volts.

12. The method of claim 1, wherein said device is a transistor and said dielectric layer is a gate insulation layer for said transistor.

13. The method of claim 1, wherein said dielectric layer is an interlevel or intralevel dielectric layer of a conductive interconnection structure.

14. The method of claim 1, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said determined time-to-breakdown.

15. The method of claim 14, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.

16. The method of claim 14, wherein determining said at least one parameter comprises determining at least one of a temperature, a pressure, a duration, a process gas composition, a process gas concentration, and an applied voltage of said at least one process operation.

17. The method of claim 14, wherein said at least one process operation comprises at least one of a deposition process, a thermal growth process and a nitridation process.

18. The method of claim 1, wherein said device is part of a test structure formed on a semiconducting substrate.

19. A method, comprising:

providing a device having a dielectric layer;

applying a plurality of constant voltage pulses to said device; and

measuring a current through said dielectric layer after one or more of said constant voltage pulses has been applied.

20. The method of claim 19, further comprising determining a breakdown point for said dielectric layer based upon said measured current.

21. The method of claim 19, further comprising determining a time-to-breakdown for said dielectric layer based upon a number of pulses applied to said device until said dielectric layer breaks down.

22. The method of claim 19, wherein said device is comprised of at least one of a transistor, a capacitor, a resistor and a memory cell.

23. The method of claim 19, wherein said dielectric layer is an interlevel or intralevel dielectric layer of a conductive interconnection structure.

24. The method of claim 19, wherein said dielectric layer is comprised of silicon dioxide or a material having a dielectric constant greater than 5.

25. The method of claim 19, wherein said constant voltage pulses have a voltage that ranges from approximately 4-5 volts.

26. The method of claim 19, wherein said pulses have a constant pulse width.

27. The method of claim 19, wherein said pulses have a constant pulse width of less than 1 μsec.

28. The method of claim 19, wherein said pulses have a constant pulse width of approximately 100 ns.

29. The method of claim 19, wherein said step of measuring said current through said dielectric layer is performed after each of said plurality of pulses.

30. The method of claim 19, wherein said step of measuring said current through said dielectric layer is performed using an applied voltage of approximately 1-2 volts.

31. The method of claim 19, wherein said device is a transistor and said dielectric layer is a gate insulation layer for said transistor.

32. The method of claim 21, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said determined time-to-breakdown.

33. The method of claim 32, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.

34. The method of claim 32, wherein determining said at least one parameter comprises determining at least one of a temperature, a pressure, a duration, a process gas composition, a process gas concentration, and an applied voltage of said at least one process operation.

35. The method of claim 32, wherein said at least one process operation comprises at least one of a deposition process, a thermal growth process and a nitridation process.

36. The method of claim 19, wherein said device is part of a test structure formed on a semiconducting substrate.

37. A method, comprising:

providing a device having a dielectric layer;

applying a plurality of constant voltage pulses to said device, each of said pulses having a constant pulse width; and

measuring a current through said dielectric layer after each of said constant voltage pulses has been applied.

38. The method of claim 37, further comprising determining a breakdown point for said dielectric layer based upon said measured current.

39. The method of claim 37, further comprising determining a time-to-breakdown for said dielectric layer based upon a number of pulses applied to said device until said dielectric layer breaks down.

40. The method of claim 37, wherein said device is comprised of at least one of a transistor, a capacitor, a resistor and a memory cell.

41. The method of claim 37, wherein said dielectric layer is an interlevel or intralevel dielectric layer of a conductive interconnection structure.

42. The method of claim 37, wherein said dielectric layer is comprised of silicon dioxide or a material having a dielectric constant greater than 5.

43. The method of claim 37, wherein said constant voltage pulses have a voltage that ranges from approximately 4-5 volts.

44. The method of claim 37, wherein said pulses have a constant pulse width of less than 1 μsec.

45. The method of claim 37, wherein each of said pulses have a constant pulse width of approximately 100 ns.

46. The method of claim 37, wherein said step of measuring said current through said dielectric layer is performed using an applied voltage of approximately 1 volt.

47. The method of claim 37, wherein said device is a transistor and said dielectric layer is a gate insulation layer for said transistor.

48. The method of claim 39, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said determined time-to-breakdown.

49. The method of claim 48, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.

50. The method of claim 48, wherein determining said at least one parameter comprises determining at least one of a temperature, a pressure, a duration, a process gas composition, a process gas concentration, and an applied voltage of said at least one process operation.

51. The method of claim 48, wherein said at least one process operation comprises at least one of a deposition process, a thermal growth process and a nitridation process.

52. The method of claim 37, wherein said device is part of a test structure formed on a semiconducting substrate.

53. A method, comprising:

providing a device having a dielectric layer;

applying a plurality of constant voltage pulses to said device, each of said pulses having a constant voltage that ranges from approximately 4-5 volts and a constant pulse width that is less than 1 μsec; and

measuring a current through said dielectric layer after each of said constant voltage pulses has been applied.

54. The method of claim 53, further comprising determining a breakdown point for said dielectric layer based upon said measured current.

55. The method of claim 53, further comprising determining a time-to-breakdown for said dielectric layer based upon a number of pulses applied to said device until said dielectric layer breaks down.

56. The method of claim 53, wherein said device is comprised of at least one of a transistor, a capacitor, a resistor and a memory cell.

57. The method of claim 53, wherein said dielectric layer is an interlevel or intralevel dielectric layer of a conductive interconnection structure.

58. The method of claim 53, wherein said dielectric layer is comprised of silicon dioxide or a material having a dielectric constant greater than 5.

59. The method of claim 53, wherein each of said pulses have a constant pulse width of approximately 100 ns.

60. The method of claim 53, wherein said step of measuring said current through said dielectric layer is performed using an applied voltage of approximately 1-2 volts.

61. The method of claim 53, wherein said device is a transistor and said dielectric layer is a gate insulation layer for said transistor.

62. The method of claim 54, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said time-to-breakdown.

63. The method of claim 62, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.

64. The method of claim 62, wherein determining said at least one parameter comprises determining at least one of a temperature, a pressure, a duration, a process gas composition, a process gas concentration, and an applied voltage of said at least one process operation.

65. The method of claim 62, wherein said at least one process operation comprises at least one of a deposition process, a thermal growth process and a nitridation process.

66. The method of claim 53, wherein said device is part of a test structure formed on a semiconducting substrate.

67. A method, comprising:

providing a plurality of devices, each of which have a dielectric layer;

applying a plurality of constant voltage pulses to each of said devices;

for each of said plurality of devices, measuring a current through said dielectric layer after one or more of said constant voltage pulses has been applied; and

determining a time-to-breakdown for each of said dielectric layers based upon a number of pulses applied to each of said devices until said dielectric layer breaks down.

68. The method of claim 67, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said determined time-to-breakdown.

69. The method of claim 68, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.

70. The method of claim 69, wherein said voltage pulses have a constant width that is less than 1 μsec.

71. A method, comprising:

providing a plurality of devices, each of which have a dielectric layer;

applying a plurality of constant voltage pulses to each of said devices, each of said pulses having a constant pulse width;

for each of said plurality of devices, measuring a current through said dielectric layer after each of said constant voltage pulses has been applied; and

determining a time-to-breakdown for each of said dielectric layers based upon a number of pulses applied to each of said devices until said dielectric layer breaks down

72. The method of claim 71, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said determined time-to-breakdown.

73. The method of claim 72, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.

74. A method, comprising:

providing a plurality of devices, each of which have a dielectric layer;

applying a plurality of constant voltage pulses to each of said devices, each of said pulses having a constant voltage that ranges from approximately 4-5 volts and a constant pulse width that is less than 1 μsec;

for each of said plurality of devices, measuring a current through said dielectric layer after each of said constant voltage pulses has been applied; and

determining a time-to-breakdown for each of said dielectric layers based upon a number of pulses applied to each of said devices until said dielectric layer breaks down

75. The method of claim 74, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said determined time-to-breakdown.

76. The method of claim 75, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.